APPLICATION
NOTE

AP-164

November 1983

Using CMOS Minimizes Bubble Memory Power Consumption

Peggy M. Lammer
Ulmont Smith, Jr.
Applications Engineers
Intel Corporation

ORDER NUMBER: 230826-001

INTRODUCTION

More and more microprocessor systems are becoming portable. Quite frequently, portable systems run on a limited power budget with a battery power supply. Others need to limit how much power they dissipate because their small enclosures dissipate only a limited amount of heat. When designing portables or any piece of processor controlled equipment, consider using bubble memories for mass storage. Bubble memories are solid state, rugged, reliable, and very small; a complete 128 kbyte bubble memory system will occupy less than a 10 cm x 10 cm area of board space. In addition, bubble memories are non-volatile; the memories still maintain their data integrity even if they are powered down to save energy when the processor is not accessing them.

To minimize a low power project's design time, part of the application note is a completely designed CMOS controlled switch that will power-down a bubble system when it is not being accessed. The switch is inexpensive and can reduce your standby power dissipation up to 99%.

OVERVIEW

This application note provides information on low power techniques for bubble memories. All the techniques can be incorporated into your existing bubble memory system with very little effort or expense. A large part of the note focuses on power switching because it is easy to add the extra hardware, and power switching offers the greatest amount of average power savings. For the moment you should know that power switching is supplying the bubble with power only when it is interacting with the host processor and removing the bubble system's power supply when the bubble is not in use.

There are two main parts to the application note. The first will explain why average power dissipation will vary with the frequency of bubble activity. Reading this section will give you an idea of how much power can be saved compared to your present operation.

The second part starts by covering some hardware considerations for power switching bubble memories. It then describes a power switching circuit designed to these considerations. In addition, this section discusses some software techniques and a secondary hardware technique called detector switching that will further reduce average power dissipation.

MEMORY ACTIVITY LEVELS AND POWER DISSIPATION

The bubble memory already reduces its power dissipation by only creating magnetic fields to move the bubbles when data is being accessed. When data is not being transferred, the magnetic fields need not be present, i.e., the coil drive currents which create the fields are removed and less power is dissipated. Table 1 is a break down of power dissipation by component for the Intel one bubble memory system in Figure 1. A system consists of a 7220 bubble memory controller and up to eight BPK-70 memory cells; a cell is a bubble memory and its support ICs.

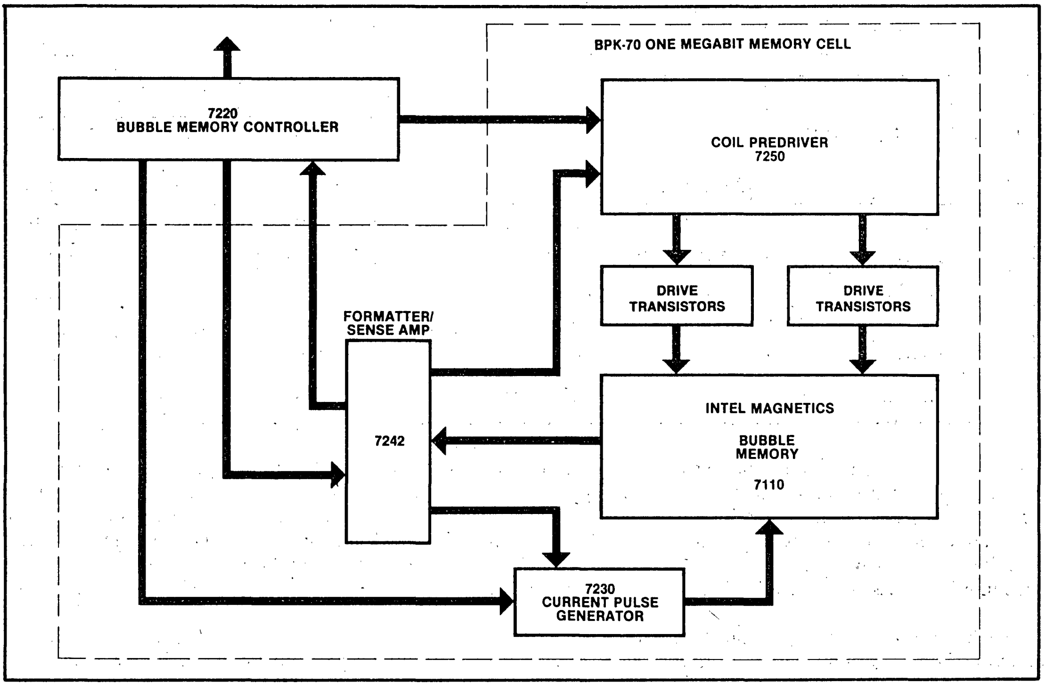


Figure 1. Bubble Memory System Block Diagram

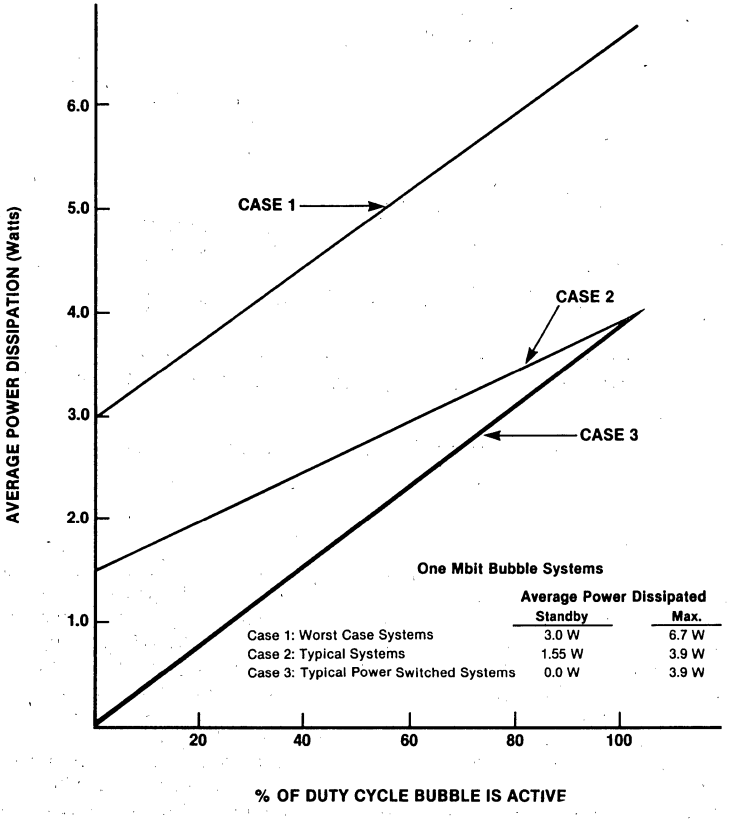
Table 1. Bubble Memory Power Requirements

Configuration		Power (Watts)					
BPK70	Capacity (Bytes)	+5V (Maximum)	+12V (Maximum)	Total Active (Maximum)	Total Active (Typical)	Total Standby (Maximum)	Total Standby (Typical)
1	128K	1.92	4.80	6.72	3.90	3.03	1.55
2	256K	2.79	9.60	12.39	7.30	4.57	2.60

Breakdown by Device	Power (Watts)					
	+5V (Maximum)	+12V (Maximum)	Total Active (Maximum)	Total Active (Typical)	Total Standby (Maximum)	Total Standby (Typical)
7110	0	1.740	1.740	1.480	0.440	0.290
7220	1.050	0	1.050	0.500	1.050	0.500
7230	0.235	0.440	0.675	0.390	0.475	0.225
7242	0.630	0.375	1.005	0.500	1.005	0.500
7250	0	0.945	0.945	0.480	0.060	0.030
7254(2)	0	1.300	1.300	0.550	0	0

Without a power switch, a bubble system not being accessed (in standby mode) will dissipate an average of 1.55 watts, 3.0 W worst case. When the host processor does access the memory, (i.e. the coils have a current running through them) the power dissipation increases to 3.9 W typically, 6.7 W worst case. Obviously, since the bubble system does nothing but dissipate 1.55 W in standby mode, it would be ideal to shut it off and dissipate zero watts. That is the purpose of a power switch. For example, the CMOS controlled switch in this note reduces standby power consumption to less than 25 mW. That is a 99% decrease in standby power consumption compared to worst case.

Figure 2 is a graph showing memory activity levels versus average power dissipation. On the graph, the average amount of time the bubble is active is represented as a percentage of duty cycle. Duty cycle is a ratio of the amount of time the bubble is active to the total time spent in standby and active modes. There are three types of systems plotted on the graph. Case 1 is worst case bubble memory systems. Case 2 represents typical systems and case 3 is typical power switched systems.



One Mbit Bubble Systems

	Average Power Dissipated	
	Standby	Max.
Case 1: Worst Case Systems	3.0 W	6.7 W
Case 2: Typical Systems	1.55 W	3.9 W
Case 3: Typical Power Switched Systems	0.0 W	3.9 W

Figure 2. A Comparison of Bubble Memory Activity to the Amount of Average Power Dissipated by the Bubble Memory System

The lowest value on each plot is the power that system dissipates in standby mode. The maximum point is the power that would be dissipated if the processor was dedicated to accessing the bubble memory continuously. To give an example of an application that falls somewhere between the extremes, consider a processor monitoring vintage wine cellars. It runs a program which collects data about the cellars' environmental conditions and stores the information in the bubble memory. Figure 3 shows how power is dissipated by a typical bubble system in two minutes assuming that the program accesses the memory for an average of six seconds when it stores data.

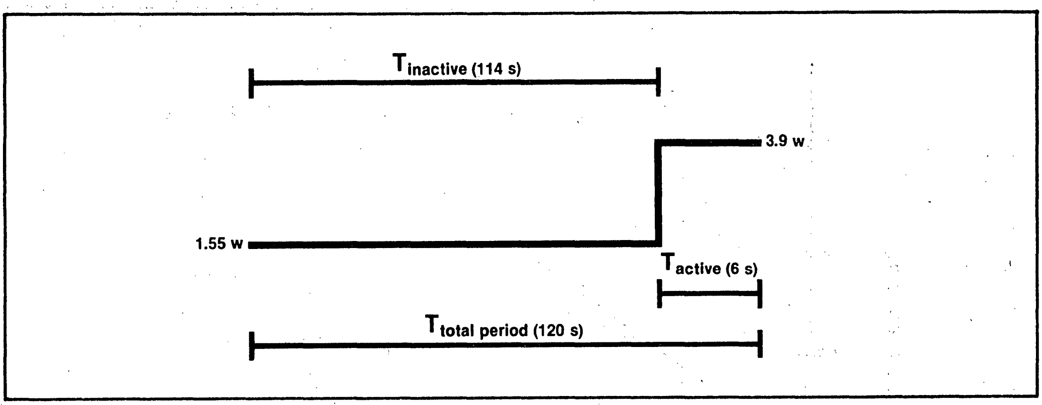


Figure 3. A Duty Cycle Period for a Bubble System with Typical Power Dissipation (Not drawn to scale)

There are two ways to figure how much average power is dissipated in the monitor example. By calculating the average,

(6s (3.90W) + 114s (1.55W)) / 120s = 1.66W

or by using the graph of Figure 2. To use the graph, the duty cycle must be calculated; six seconds is 5% of 120 seconds. After finding 5% on the % duty cycle axis, the amount of power dissipated can be read off the typical system plot. It is also interesting to note how much power would have been dissipated had the bubble system been worst case or power switched. Those values are 3.15 W and 0.35 W respectively; switching time overhead was neglected. If the monitor was to run on a battery for long periods of time, the graph indicates that it would be very worthwhile to add a power switch, about 1.40 W saved per minute over worst case design.

Generally, your duty cycle will be well below 20%. Data acquisition, portable terminal and portable PC applications have long term duty cycles of less than 10%. Even in a high transaction rate application the duty cycle is frequently small. For instance, the processor in a grocery store's point of sale terminal accesses a bubble system for information on items as often as every second. If the information can be read out in 256 byte blocks, then it will take the bubble approximately 63.5 ms to access the data, yet the duty cycle is still only about 6%, (63.5 ms/ 1 s) x 100% ~ 6%.

If your data access and standby times vary, you will want to estimate your average duty cycle so you can use the graph to determine how much power could be saved by switching the bubble. A bubble will take about 41 ms to locate specific memory locations and then it can transfer consecutive pages of 64 bytes approximately every 7.5 ms. Estimate your active unswitched time as follows,

.041s + .0075s (NUMBER OF PAGES TO TRANSFER) = ACTIVE TIME (seconds)

A switched system will have a slightly greater active time due to switching overhead,

Power-up Time + ACTIVE TIME + Power-down Time = ACTIVE TIME (switched)

This incremental difference is not neglible if ACTIVE TIME is very small. For example, the switch documented in the note takes 160 ms to power-up and 48 ms to power-down. If the grocery store's point of sale terminal used that power switch then its active time would change from 6% to 27%. From the graph, the difference in average power dissipation is .76 W, (1.8 W — 1.04 W). Switching is not recommended for systems with average duty cycle periods of less than one second.

LOW POWER DESIGN TECHNIQUES

The most efficient way to reduce your bubble system's average power consumption is to turn off the bubble when it is not being used by the processor. Designing in the simple switch documented in this section will do this quickly. All the hardware considerations necessary to successfully power switch a bubble system are included.

Two other topics will be discussed besides power switching, a secondary hardware switch for the bubble memory's detector and some software considerations including the fastest way to initialize a power switched bubble system and some software considerations such as the fastest way to initialize a power switched bubble system and some energy efficient software techniques for bubble memories in general.

HARDWARE CONSIDERATIONS FOR POWER SWITCHES

This is a basic outline of what is involved in power switching a bubble system. It is not a very complicated process. The CMOS controlled switch or one of your own design can be added in with very little system modification. Figure 4 is a block diagram of how the interface between your bubble memory and host processor will look with the sample switch in place. A table of typical values measured when the switch was validated appears in the appendix.

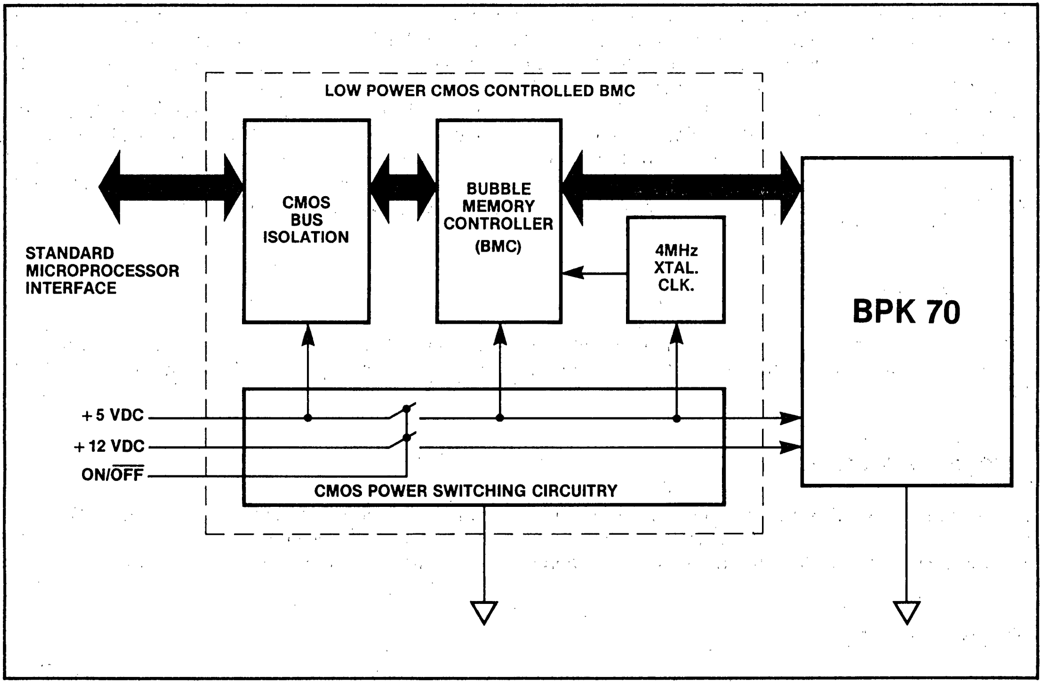

LOW POWER CMOS CONTROLLED BMC
STANDARD MICROPROCESSOR INTERFACE
CMOS BUS ISOLATION
BUBBLE MEMORY CONTROLLER (BMC)
4MHz XTAL. CLK.
BPK 70
+5 VDC
+12 VDC
ON/OFF
CMOS POWER SWITCHING CIRCUITRY

Figure 4. Block Diagram of a Low Power Bubble Memory System

Integrating A Power Switch To A Bubble Memory

There are two power supplies to the bubble system that will need to be disconnected when the bubble is in standby mode. They are +5 Vdc and +12 Vdc respectively. In addition to supplying these voltages within a ±5% voltage tolerance, the switch must also comply with the power-down specifications for Intel bubble systems. The power-down decay rates are;

Power on the 5 Vdc line must not decay at a rate exceeding 0.45 V/ms.

Power on the 12 Vdc line must not decay at a rate exceeding 1.10 V/ms.

These rates must be maintained for 120 μs after the 7220 bubble memory controller (BMC) recognizes that a power-down has occurred; for more information on power-downs, see Application Note 127, Powerfail Considerations for Magnetic Bubble Memories.

In any case, the power switch circuit described in this note maintains a 150 μs delay for itself on either a controlled power-down or on complete system power loss. The incorporated delay allows the switch to be swiftly integrated into any existing memory system whose supplies already comply with the decay rates.

Aside from the switch interface, the BMC will do its communications directly with the host processor. During power-ups and downs, these two technically sophisticated devices need to be isolated from each other so that neither one sends destructive noise to the other (the BMC in particular should not see any inputs greater than V_{CC} + 0.5 Vdc at anytime). This isolation can be accomplished with bus transcievers which maintain a large impedance between the devices. The transcievers will also add a round trip delay to the bus signals, and that delay should be added to the read and write strobes, RD/ and WR/. For example, the transcievers used in the sample switch have a round trip delay of 100 ns worst case so the two strobes should be increased from 200 ns to 300 ns. In low power systems, 300 ns strobes are not uncommon and system performance should not be compromised. A typical case, the Intel 8088 Microprocessor running at 5 MHz will still have a read strobe in excess of 300 ns.

Bubble System Clock

The BMC needs a 4 MHz, TTL level clock to do self-contained timing. The clock generator will have to be switched with the bubble memory system. Again, this is to prevent signals larger than V_{CC} +0.5 Vdc from being sent to the BMC.

Selecting Components

Selected parts should dissipate a minimum amount of power or the switch will defeat its own purpose. When the sample switch was prototyped, several CMOS components were picked because of their low power CMOS characteristics. In particular, the transcievers are compatible with either a 5 Vdc CMOS or TTL processor bus.

Switch Selection

A bubble system power switch should be as fast and reliable as the bubble system, have a small 'on' resistance, and be able to operate using the existing power supplies. There are two choices for switches, relays and FETs. FETs were chosen over relays for the prototype switch because they are faster and more reliable. Frequently, mechanical relays do not have lifespans comparable to bubble memory systems.

An N-channel FET was used on the 5 Vdc supply line. NFETS have low 'on' resistances and are for the most part inexpensive. By connecting a 5 Vdc supply to the NFET drain, a nominal 5 Vdc can be supplied to the bubble by the source terminal when Vgs is large enough to turn on the NFET. The switch is turned on and off by changing the gate voltage, Vg, from 12 Vdc to 0.0 Vdc. When Vg is 12 Vdc, Vgs is 7 Vdc and the NFET is on; zero volts at Vg does not create a large enough Vgs to turn the NFET on.

In a similar way, a PFET on the 12 Vdc line supplies the bubble system with a nominal 12 Vdc supply. An NFET was not used because it would require 19 Vdc at the gate to set Vgs to 7 Vdc and have the FET turn on. Instead Vg switches from 0.0 Vdc to 12 Vdc.

Although the voltage drops across the FETs will be very small, they will add incrementally to the amount the bubble supplies vary from their specified voltages. For example, if the switch has a −1.5% voltage drop across it and your power supplies vary by ±3.5%, then the total operating range for the bubble's supplies is −5% to +2% nominal which is still within specifications. However, if your supplies varied by ±4%, then the bubble supplies would be out of specification by 0.5% on the low margin. To always stay within specification, operate your power supplies slightly off-set into their high margins. This procedure is not necessary, but it does add some operating margin to the system.

For example, in the sample switch the NFET for the 5 Vdc line has a worst case 'on' resistance of 0.16 ohms (@ 75 °C). The 12 Vdc line's PFET has 0.40 ohms (@ 75 °C) of 'on' resistance.

Using Table 1 the maximum power supply currents can be calculated,

Vd = +5 Vdc; 384 mA
Vs = +12 Vdc; 400 mA

and the worst case voltage drops across the FETs are then,

(+5 Vdc) Vds = (384 mA) 4) (0.16 ohms) = 62 mV
(+12 Vdc) Vds = (400 mA) (0.40 ohms) = −160 mV

Finally, the operating margins will change by,

(+5 Vdc) (62mV/5V) 100% = 1.24%;
+6.24% to −3.76% = operating margin
(+12 Vdc) (160 mV/12V) 100% = 1.33%;
+6.33% to −3.67% = operating margin

Doing a similar analysis for two bubble system with only one bubble active at anytime yields these operating margins,

(+5 Vdc) +6.79% to −3.21%
(+12 Vdc) +6.75% to −3.25%

A POWER SWITCH

Some characteristics of the CMOS controlled power switch shown in Figure 5 have already been described. To reiterate, the switch is easy to assemble and should require little if any system modifications. A user will have only one bus signal to indicate power on or off to the switches, (there is also an optional interrupt line to signal the processor that the supplies are operational, i.e., above powerfail threshold levels). The circuit itself is low power (25 mW standby max.) and has reliability compatible with the bubble memory system. Finally, unlike disks whose mechanical latency make them difficult to switch, the switch and the bubble system are all solid state so frequent switching can be accomplished rapidly.

A TTL or CMOS processor using DMA or polled data transfer modes with a bubble system (two bubble memories maximum) can handle this switch.

Driving The FET Switches

The one bus signal from the processor to the switch in Figure 5 is called POWER-ON. To supply power to the bubble system, POWER-ON is set active high; a logic low on POWER-ON signals a power-down.

POWER-ON is fed to the positive inputs of two comparators with open collector outputs; both negative inputs are set to 1.5 Vdc, i.e., POWER-ON signals greater than 1.5 Vdc are considered logic highs. The output of one comparator is sent to the BMC's RESET/ input. RESET/ is the BMC's hard reset signal. When it goes active low, it is an indication to the BMC that a power-down is occurring.

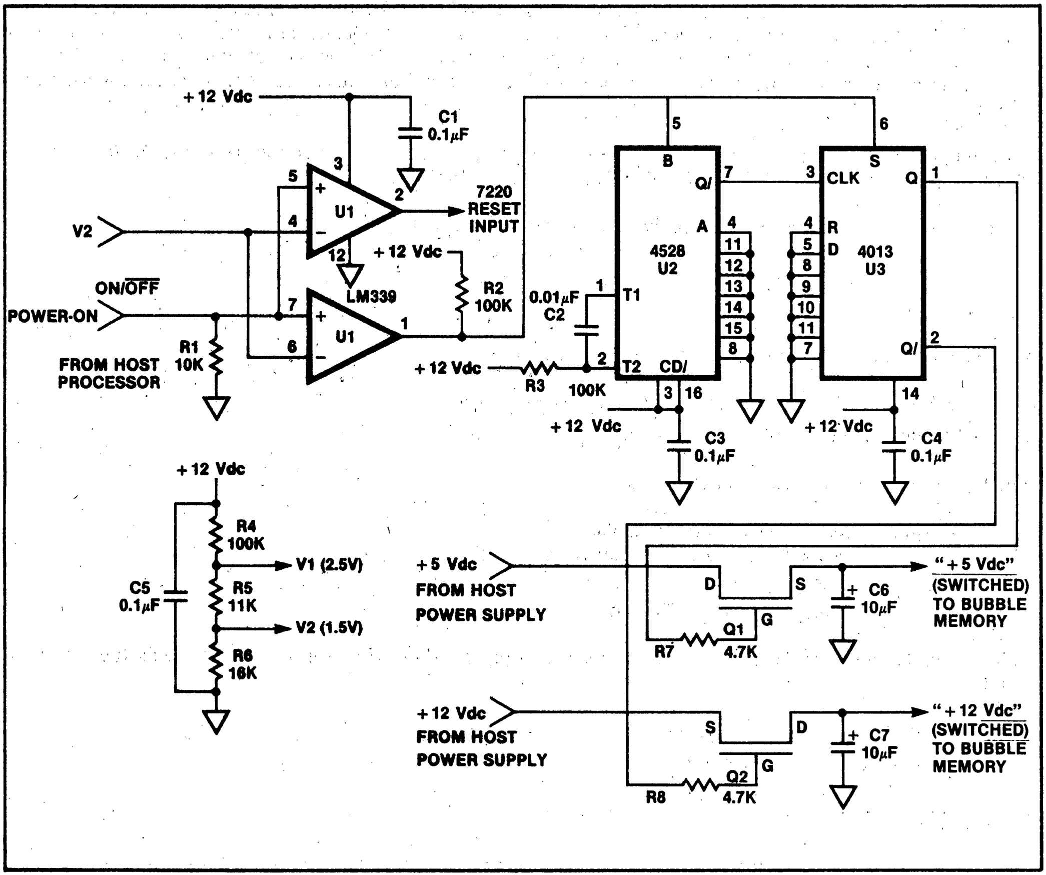


Figure 5. Bubble Memory Power Supply Switching Circuitry

Table 2. Parts List

Part	Purpose
	ALL RESISTORS ARE 0.25 W. 5% TOLERANCE.
R1 = 10 kohms	Sets gate input to low in absence of a drive signal.
R2 = 100 kohms	CMOS pull-up resistors.
R3 = 100 kohms	Sets 150 μs or greater time cosntant delay for one-shot.
R4 = 100 kohms	Voltage divider (Establishes V1 and V2 references).
R5 = 11 kohms	Voltage divider (Establishes V1 and V2 references).
R6 = 16 kohms	Voltage divider (Establishes V1 and V2 references).
R7, R8 = 4.7 kohms	Controls transition rate of Vs and Vd.
R9, R10 = 5.1 kohms	CMOS pull-up resistors.
C1, C3, C4, C5, C8, 0.1μF, 50 VDC	Power supply decoupling capacitors.
C2 = .01μF (typical) 50 VDC	Sets 150 μs or greater time constant delay for one-shot.
C6, C7 5 10 μF, 25 VDC	Power supply decoupling capacitors.
U1	LM339 low power quad comparator.
U2	4528 CMOS dual one-shot.
U3	4013 CMOS dual D flip flop.
U4, U5	74SC245 CMOS octal transcievers.
U6	74LS08 AND gate.
Q1	Siemens N-channel Econofet, BUZ71A
Q2	International Rectifier P-channel FET, IRF9531
Q3	N-channel FET, 2N6659 (Optional 7110 Bubble Memory Detector Switching)

The other comparator's output, herein referred to as Vo, is tied high to 12 Vdc through 100 kohms. It controls two CMOS components, a D flip flop through its SET input and a one-shot through its trigger input. While Vo remains high, the flip flop's outputs will remain set (Q equals +12 Vdc and Q/ equals 0.0 Vdc) since SET, equal to Vo, will be high, 12 Vdc. The outputs, Q and Q/, are connected to the FET gates through 4.7 kohm resistors; Q drives the NFET's gate on the 5 Vdc line and Q/ drives the PFET on the 12 Vdc line. The resistors are in series with the FETs' internal capacitances and are used to control the rate at which the supplies power-up and down.

When POWER-ON goes to logic low, the output connected to RESET/ will cause the BMC to start its internal power-down routine. It will now take the BMC 120 μs (worst case) to execute an orderly shut down. During this time, the power-down decay rate specified in the hardware considerations section MUST BE SUPPORTED or data integrity may be compromised.

The power switch keeps the supply lines open by keeping the FETs on until 150 μs have elapsed after POWER-ON goes low. Vo will follow POWER-ON as it goes from logic high to logic low. The one-shot will trigger off Vo's falling edge. After waiting 150 μs, the output from the one-shot will clock the D flip flop and Q and Q/ will be reset. This resets the NFET's gate voltage to 0.0 V and the PFET's to 12 Vdc. Now both FETs are off, i.e., so are the bubble system's power supplies.

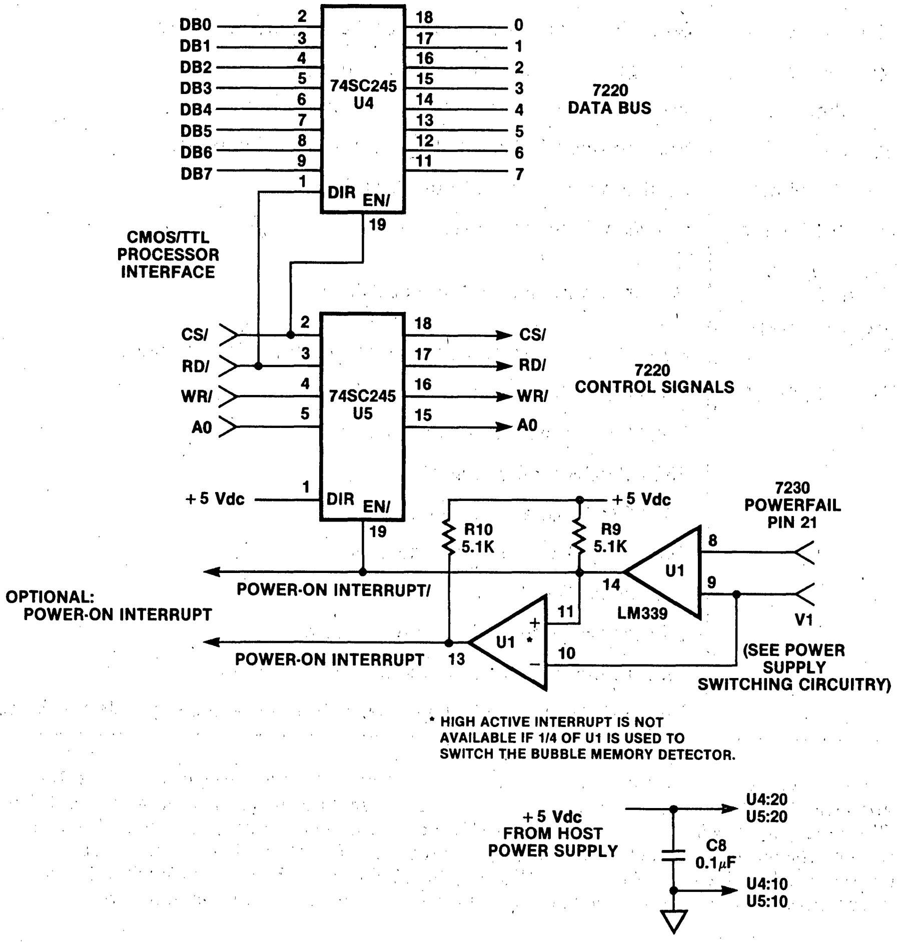


Figure 6. Bubble Memory Power Switch CMOS Bus Isolation Circuitry Polled Mode Only

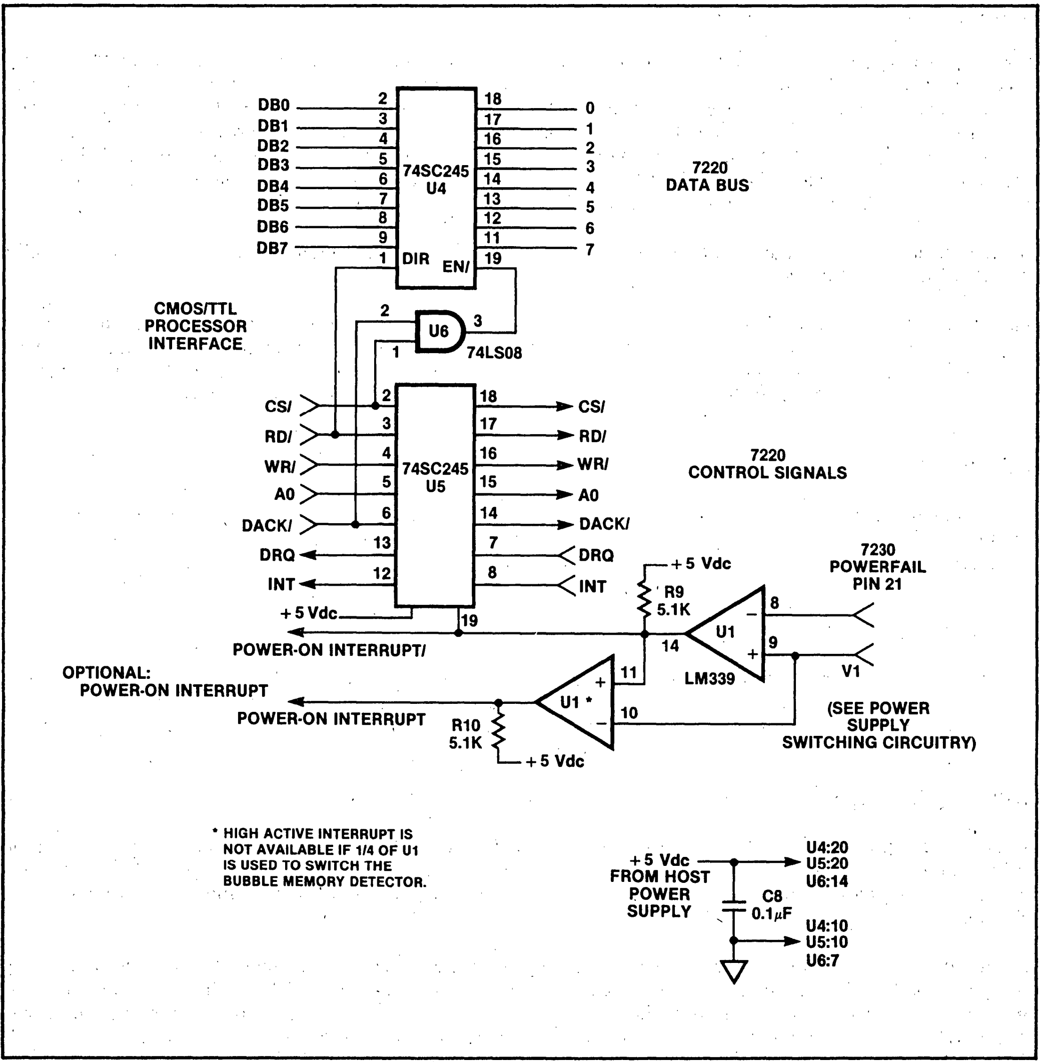


Figure 7. Bubble Memory Power Switch CMOS Bus Isolation Circuitry Polled/DMA Mode

Enabling The Interface Bus

Once the power supplies are operational, the switching circuit will enable the interface bus. Figures 6 and 7 are two possible designs for the bus transcievers; Figure 6's circuit supports polled data transfers only, Figure 7 is a modified version of Figure 6 which supports either polled or DMA. Both designs use the open collector output of a comparator to enable the BMC control signals; the output is tied high to 5 Vdc via 5.1 kohm resistors. The inputs to the comparator are 2.5 Vdc on the positive input and the 7230 current pulse generator's powerfail output, PWR.FAIL/ (pin 21), is sent to the negative input. When PWR.FAIL/ is high, greater than 2.5V, the bus is enabled, and an active low PWR.FAIL/ signal would disable the bus.

The data bus lines are not enabled until the processor selects the bubble system to do a data transfer by setting CS/ (or DACK/ for DMA) active low.

As an option, bus the output signal of the PWR.FAIL/ comparator to the host processor for an interrupt to detect when the power supplies are operational. Otherwise the processor will have to delay interacting with the bubble system until the supplies can be guaranteed operational. Invert the interrupt line with the unused fourth comparator if your processor supports active high interrupts; PWR.FAIL/ is active low on a power-down.

SOFTWARE CONSIDERATIONS

All the software information needed to successfully power switch a bubble system is presented here. Application Note 157, Software Design and Implementation Details for Bubble Memory Systems, is a useful reference if you are unfamiliar with the fundamentals of bubble memory software.

Data Transfer Modes

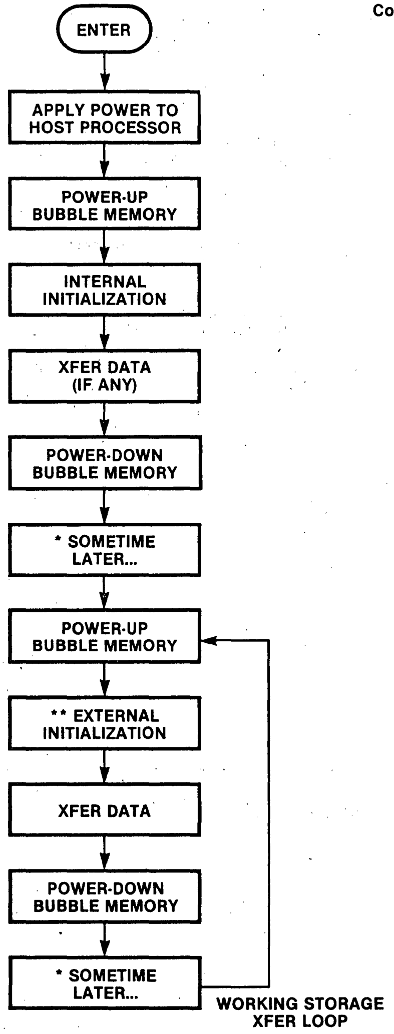
Two data transfer modes compatible with the switching circuit's bus interface are polled and DMA. Polled mode is easy and consumes the least amount of power and board space. DMA requires a DMA controller and the BMC's DRQ, DACK/ and INT signals are added to the bus interface.

Initializing The Bubble Memory

An initialization procedure must be followed after every power-up to place the BMC in a known state, to load the bootloop code into the bootloop registers and to synchronize the bubble memory to its first logical page of 64 bytes. In power switched systems, power-ups will occur before each memory access and a fast initialization routine is very desirable.

There are two ways to initialize a bubble memory. One is an internally generated command sequence executed by sending the INITIALIZE command to the BMC. The other method emulates INITIALIZE by sending the command sequence and bootloop code from the host processor to the BMC, but does not synchronize the bubble memory. This external initialization does have the advantage of being faster; worst case execution of an INITIALIZE command is 170 ms versus 5 ms for an external initialization.

Both types of initialization should be used in a power switched configuration. Send an INITIALIZE command after every cold start to synchronize the bubble memory. At the completion of the data transfer, have the BMC execute a WRITE SEEK to location (page) 395H or a READ SEEK to location 9BH. This will synchronize the bubble as the INITIALIZE command did. The bubble is non-volatile so this synchronization will not be lost even when power is removed. On the next and subsequent power-ups, use the external initialization to quickly put the BMC into a known state and place the bootloop code into the bootloop registers. Then continue to do a seek operation on each power-down to keep synchronization. Figure 8 flowcharts the operating sequence just described for low power bubble memory systems. Figures 9 and 10 are the power-up and down sequences. Flowcharts for the internal and external initialization routines are in the appendix.



Comments: The sequence of events outlined in the flowchart must be executed each time the host processor is powered-up.

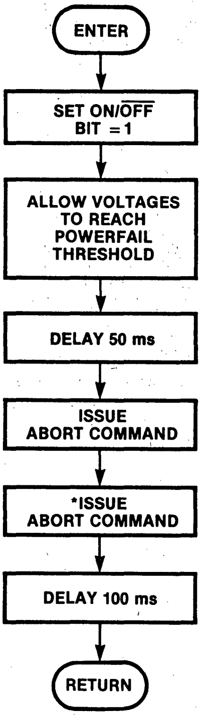
* The typical time between removing the power from a Bubble Memory to powering back up should be approximately one second or greater to derive the maximum benefits from power switching.

** An external initialization is used to decrease the power-up overhead time from 235 ms with an internal initialization to less than 160 ms. However, in all cases, an internal intitialization can be substituted for an external intitialization to accommodate existing software.

Additional detail can be found in the following flowcharts:

A. Powering-Up A Bubble Memory, Fig. 9
B. Powering-Down A Bubble Memory, Fig. 10
C. Internal Initialization, Fig. 13
D. External Initialization, Fig. 14

Figure 8. Low Power Bubble Memory System Flowchart


ENTER
SET ON/$\overline{\text{OFF}}$ BIT =1
ALLOW VOLTAGES TO REACH POWERFAIL THRESHOLD
DELAY 50 ms
ISSUE ABORT COMMAND
*ISSUE ABORT COMMAND
DELAY 100 ms
RETURN

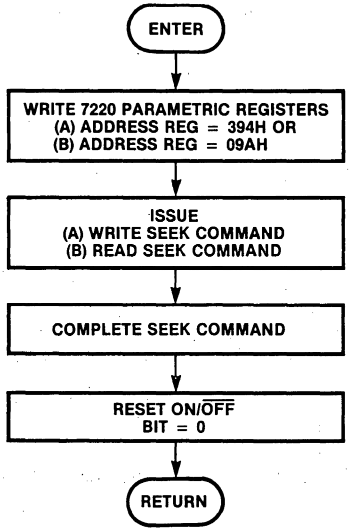
Comments: An optional Power-On Interrupt is available from the Bubble Memory power supply switching circuitry to detect when V_S and Vd have reached their respective threshold voltage. The interrupt can be omitted in place of an additional delay. The amount of delay is system and power supply dependent but is usually less than 5 ms.

Further detail concerning the successful execution of the Abort command can be found in Application Note 157, "Software Design and Implementation Details for Bubble Memory Systems."

* In all cases, a second ABORT command guarantees that the BMC resets.

Total execution time is typically less than 155 ms.

Figure 9. Power-up Flowchart for a Low Power Bubble Memory System



Comments: Either a Write Seek Command at address 394H or a Read Seek Command at 09AH is sufficient to synchronize the Bubble for an external initialization.

Seeking prior to powering-down is not necessary if an external initialization is not implemented.

Worst case seek time is 90 ms. Average seek time is 48 ms.

Figure 10. Power-down Flowchart for a Low Power Bubble Memory System

An easy way of keeping the bootloop code outside the bubble is to read it out of the bootloop registers, after each cold start, into the host system's RAM. Then retrieve the code from RAM for each external initialization.

The seek commands expect their operands to be the number of the page one previous to the page you wish to seek. For example, the page that should appear as the operand in the WRITE SEEK command for the initialization routine above is 394H and the READ SEEK operand should be 9AH.

If speed is not a factor, you can use the INITIALIZE command after every power-up, but the total amount of time before a data transfer can begin will still be the time it takes for the power supplies to become operational, typically 155 ms plus the time to initialize the bubble system,

Power-up + Internal Initialization = 325 ms (worst case)
Power-up + External Initialization = 160 ms (worst case)

Efficient Software

Every operation run on your system sets its own bubble memory needs. How efficiently your system responds to these needs determines how much power is dissipated. Some suggestions for energy efficient drivers and programs follow.

If information is called in a fixed sequence, store it in that fixed sequence.

Instead of repeatedly accessing the bubble for the same information, transfer the data into system RAM and retrieve it from there.

Transferring many pages of data is more efficient than doing many small transfers.

Intrinsically, running multibubble systems in serial will use less power than running parallel memories since in the former case only the coil drives of one bubble memory will be active at any one time. For example, a system running two bubbles in serial will have one active bubble memory and one bubble in standby mode any time the system is accessed. This means 5.45 W, 3.9 W + 1.55 W, will typically be dissipated during the access. Run in parallel, these same two bubbles will typically dissipate 3.9 W each or 7.8 W total during a data transfer.

DETECTOR SWITCHING

Although power switching is the primary hardware technique, the BMC has an output signal that indicates when the detector stacks are active. One advantage detector switching has over power switching is that the bubble system does not need to be reinitialized when power is reapplied.

Since the stacks are only used to sense the bubbles during read operations, the DETECTOR ON/ signal can be used to switch power to the detectors. Standby power consumption can be reduced by 20% per bubble memory if the detectors are switched off and the incremental amount you gain by leaving them off during write operations depends on the frequency and duration of your read and write operations. For example, a jet airplane's bubble memory flight recorder (using eight one mega-bit bubbles) has data written out to it on every flight. It will only be read if there is a problem during a flight. By switching off the detectors, four watts are saved on each flight (0.5 W/bubble).

Figure 11 is the circuit diagram for a detector switch. DETECTOR ON/ is inverted with a comparator; DETECTOR ON/ is the negative input, 1.5 Vdc is the positive input and the output is tied high to 5 Vdc through 100 kohms. The inverted signal is used to change an NFET's gate voltage which turns the NFET on and off. That in turn switches the detector supply on and off. Placement of the NFET is critical; lay it out as close to the bubble memory as possible.

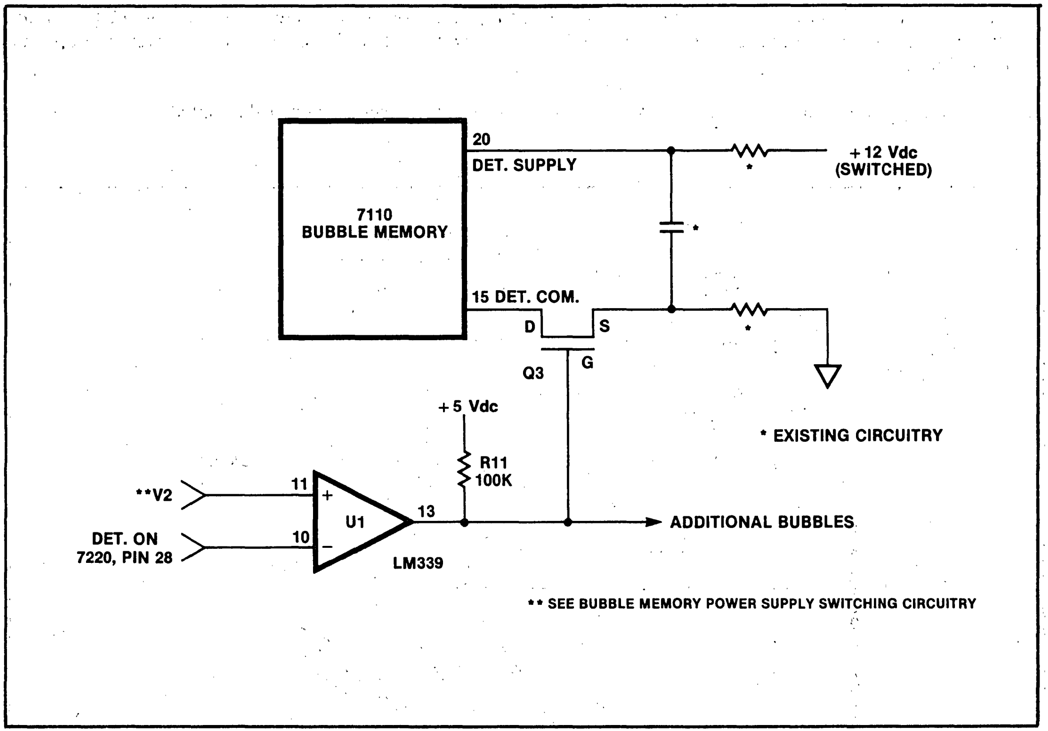
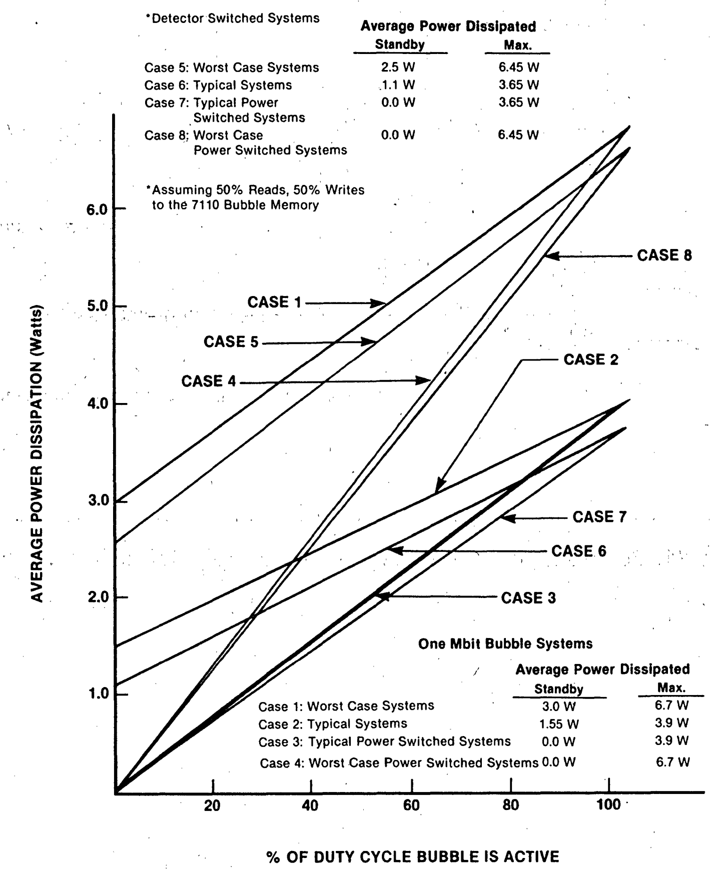


Figure 11. Bubble Memory Detector Power Supply Switching Circuitry

With a very restricted power budget, consider implementing both power and detector switching. In the sample switch, the unused fourth comparator is available for the detector switch if it is not used to invert the optional power-on interrupt.

Figure 12 is a graph comparing complete switching to the amount of average power dissipated.



*Detector Switched Systems

	Average Power Dissipated	
	Standby	Max.
Case 5: Worst Case Systems	2.5 W	6.45 W
Case 6: Typical Systems	1.1 W	3.65 W
Case 7: Typical Power Switched Systems	0.0 W	3.65 W
Case 8: Worst Case Power Switched Systems	0.0 W	6.45 W

*Assuming 50% Reads, 50% Writes to the 7110 Bubble Memory

One Mbit Bubble Systems

	Average Power Dissipated	
	Standby	Max.
Case 1: Worst Case Systems	3.0 W	6.7 W
Case 2: Typical Systems	1.55 W	3.9 W
Case 3: Typical Power Switched Systems	0.0 W	3.9 W
Case 4: Worst Case Power Switched Systems	0.0 W	6.7 W

Figure 12. A Complete Comparison of Bubble Memory Activity to the Amount of Average Power Dissipated by the Bubble Memory System

SUMMARY

The main goal of this application note is to assist designers developing portable or other low power equipment. By utilizing the CMOS controlled power switch, a designer can build a simple, reliable, low power bubble memory system with a minimum of time and effort.

APPENDIX A

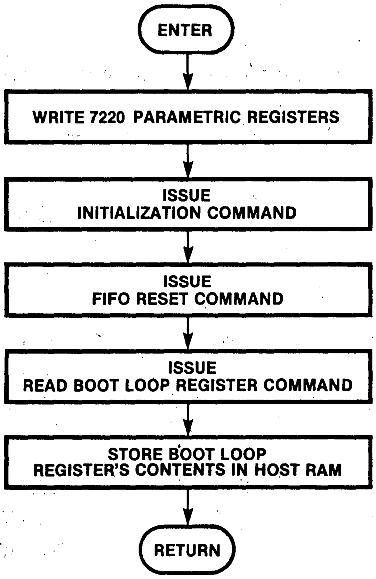
Typical Measured Values @ 25°C

Configuration — One megabit Bubble Memory System incorporating a polled mode interface.

		Vs (+5VDC)	Vd (+12VDC)
Case 1:	Power-On = Off		
	Bubble Memory System Power Consumption	0.19 mW	13.66 mW
Case 2:	Power-On = On		
	Bubble Memory in Standby		
	* Total Bubble Memory System Current	260 mA	39.4 mA
	* Bubble Memory System Power Consumption	1.3 W	0.5 W
	Voltage Drop Across the FET Switch	32.1 mV	9.5 mV
Case 3:	Power-On = On		
	Bubble Memory Actively Transferring Data		
	* Total Bubble Memory System Current	262 mA	252 mA
	* Bubble Memory System Power Consumption	1.3 W	3.0 W
	Voltage Drop Across the FET Switch	32.4 mV	61.8 mV
Power-Up Rise Time (Power-On = 1)		150 μs	600 μs
Power-Down Fall Time (Power-On = 0)		15 ms	250 ms

*Includes an Intel 8284A clock generator to produce the required 4 MHz clock for the 7220 controller and BPK-70 (7242 Formatter Sense Amplifier).

Clock Specifications:	**Parameter**	**Min.**	**Max.**
	Clock Period	249.75 ns	250.25 ns
	Clock Phase Width (High)	45%	55%
	Input Signal Rise Time		30 ns

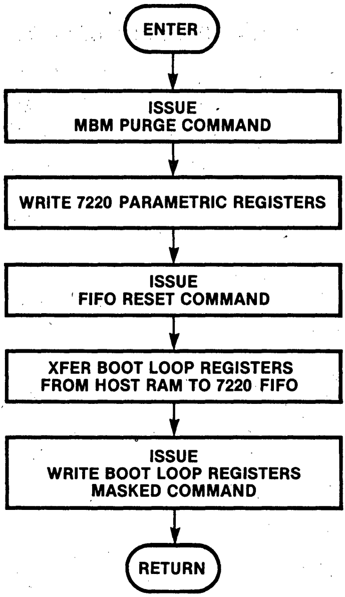

ENTER
WRITE 7220 PARAMETRIC REGISTERS
ISSUE INITIALIZATION COMMAND
ISSUE FIFO RESET COMMAND
ISSUE READ BOOT LOOP REGISTER COMMAND
STORE BOOT LOOP REGISTER'S CONTENTS IN HOST RAM
RETURN

Comments: After completing the Read Boot Loop Register Command, a copy of the Boot Loop Register is available in the 7220's FIFO. The contents of the FIFO must be stored in the host processor's RAM for later use when performing an external initialization. Transferring a copy of the Boot Loop Register is not necesary if an external initialization is not implemented.

Further detail concerning the successful execution of Bubble Memory Commands can be found in Application Note 157, "Software Design and Implementation Details for Bubble Memory Systems."

Total worst case execution time is 170 ms. Average execution time is 90 ms.

Figure 13. Internal Initialization Flowchart


ENTER
ISSUE MBM PURGE COMMAND
WRITE 7220 PARAMETRIC REGISTERS
ISSUE FIFO RESET COMMAND
XFER BOOT LOOP REGISTERS FROM HOST RAM TO 7220 FIFO
ISSUE WRITE BOOT LOOP REGISTERS MASKED COMMAND
RETURN

Comments: Total execution time is less than 5 ms.

Further detail concerning the successful execution of Bubble Memory Commands can be found in Application Note 157, "Software Design and Implementation Details for Bubble Memory Systems."

Figure 14. External Initialization Flowchart